

1/7

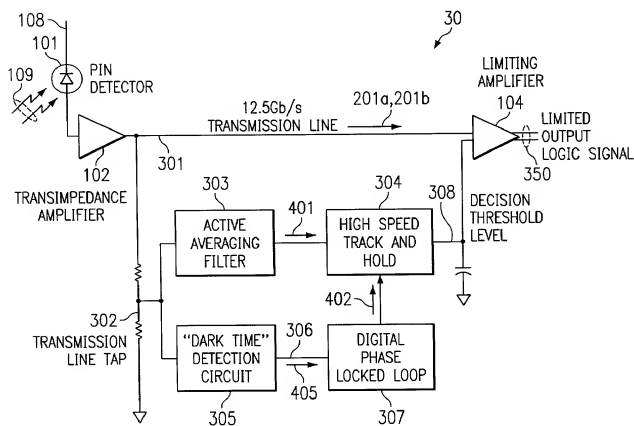
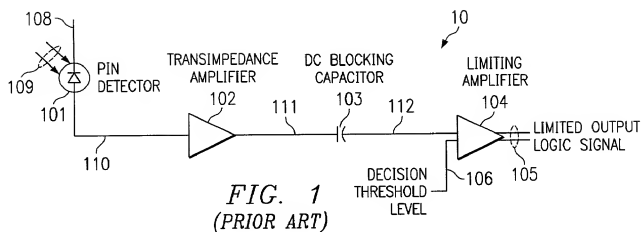


FIG. 3

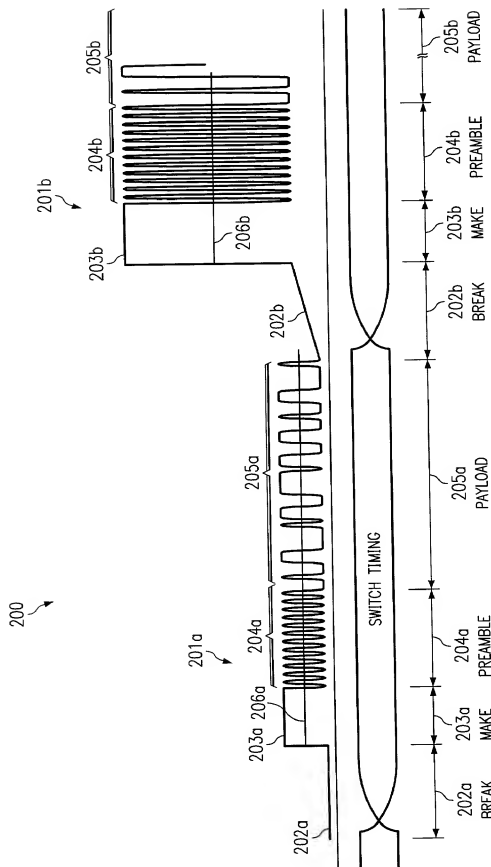
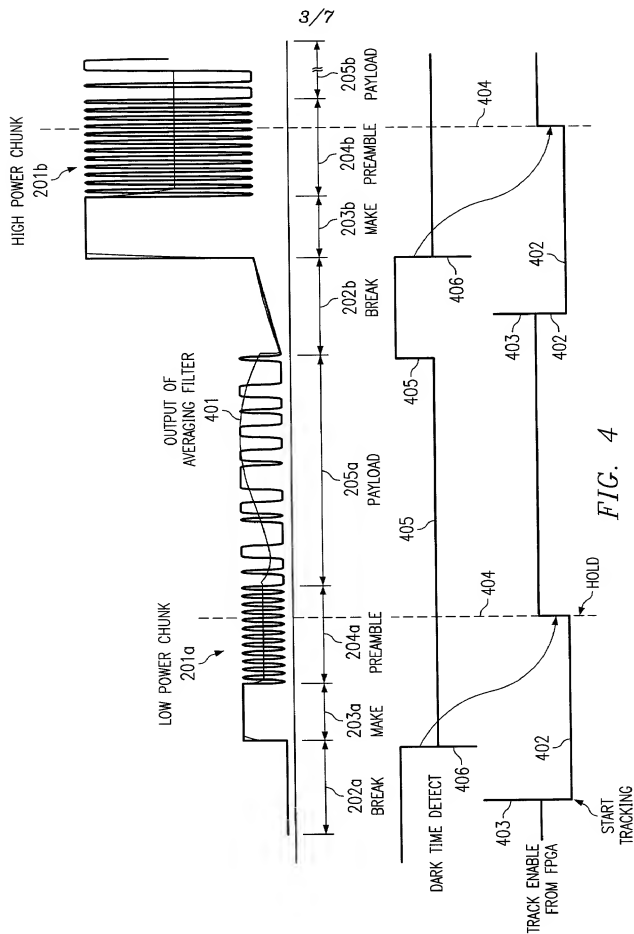
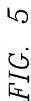


FIG. 2





The circuit diagram shows an RF line tap (302) connected to a resistor (502). The output of the resistor (502) is connected to the non-inverting input (+) of a high speed CFA amplifier (U1). The output of U1 is connected to the non-inverting input (+) of a high speed precision peak detector (U23). The output of U23 is connected to the non-inverting input (+) of a clamping amplifier (U7). The output of U7 is connected to the non-inverting input (+) of a dark time detector comparator (U4). The output of U4 is labeled "SIGNAL TO PLL". The circuit also includes a feedback loop (506) and a resistor (510) connected to the output of U4.

304

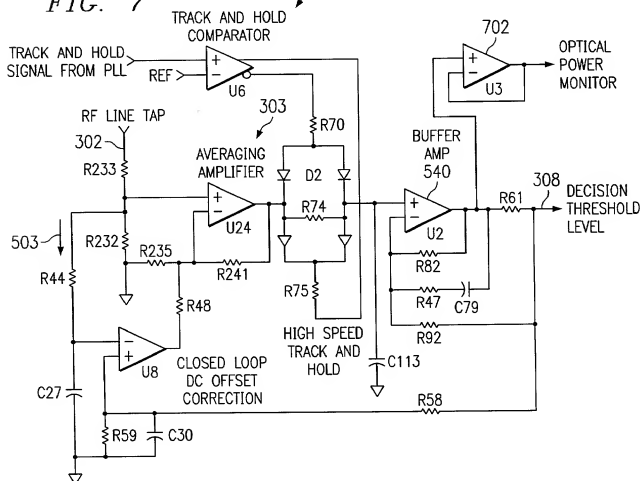




FIG. 8

FIG. 9

